What is claimed is:

1. An apparatus for forwarding data between processing elements, comprising:

a first processing element, said first processing element including an update-transmit element;

a forwarding storage element coupled to said update-transmit element; and

a second processing element coupled to said forwarding storage element, said second processing element including:

a register, and

an address register.

2. The apparatus of claim 1, wherein said forwarding storage element is a first-in first-out storage element.

3. The apparatus of claim 1, wherein said forwarding storage element is a queue.

4. The apparatus of claim 1, wherein said forwarding storage element receives a first memory address from said update-transmit element and said second processing element compares the first memory address in said forwarding storage element with a second memory address in said address register.

5. The apparatus of claim 4, wherein said second processing element stores data from said forwarding storage element to the register of said second processing element based on the comparison of the second memory address with the first memory address.

6. The apparatus of claim 1, wherein said first processing element and said second processing element is disposed within a telecommunications switch.

7. The apparatus of claim 1, wherein said second processing element stores data from said update-transmit element to the register of said second processing element.

8. The apparatus of claim 1, wherein said forwarding storage element includes a data field and an address field.

9. The apparatus of claim 1, wherein said forwarding storage element includes a last-update flag.

10. The apparatus of claim 1, wherein said forwarding storage element includes a time-to-live field.

11. The apparatus of claim 1, wherein said first processing element writes the data to memory shared by said first processing element and said second processing element.

12. The apparatus of claim 1, further comprising a shared memory.

13. The apparatus of claim 1, further comprising a third processing element coupled to said first processing element, said first processing element sending a signal to said third processing element indicating that said third processing element may access a memory shared between said first processing element and said third processing element.

14. An apparatus for forwarding data between processing elements, comprising:

a first processing element including an address register, a first memory address being stored in said address register;

a forwarding storage element coupled to said first processing element; and

a second processing element coupled to said forwarding storage element, said second processing element transmitting a second memory address to said forwarding storage element, said forwarding storage element transmitting the second memory address to said first processing element;

said first processing element comparing the second memory address with the first memory address.

15. The apparatus of claim 14, wherein said forwarding storage element stores a memory address received from said update generator.

16. The apparatus of claim 14, wherein said forwarding storage element is a first-in-first-out storage element.

17. The apparatus of claim 14, wherein said forwarding storage element is a queue.

18. The apparatus of claim 14, wherein said first processing element includes a data register, said first processing element storing data associated with a memory address from said forwarding storage element to said data register.

19. The apparatus of claim 14, wherein said first processing element includes a data register, said first processing element storing data from said forwarding storage element to said data register based on the result of the address comparison.

20. The apparatus of claim 14, wherein said update generator transmits a data value and associated memory address to said forwarding storage element

21. The apparatus of claim 14, wherein said first processing element is disposed within a telecommunications switch.

22. The apparatus of claim 14, wherein said forwarding storage element includes a data field and an address field.

23. The apparatus of claim 14, wherein said forwarding storage element includes a last-update flag.

24. The apparatus of claim 14, wherein said forwarding storage element includes a time-to-live field.

25. The apparatus of claim 14, wherein said first processing element includes said forwarding storage element.

26. The apparatus of claim 14, wherein said second processing element includes said forwarding storage element.

27. The apparatus of claim 14, wherein said forwarding storage element is separate from said first processing element and said second processing element.

28. The apparatus of claim 14, wherein said first processing element and said second processing element are included in a ring of processing elements.

29. The apparatus of claim 14, wherein said first processing element is adjacent to said second processing element in a ring of processing elements.

30. The apparatus of claim 14, further comprising a third processing element coupled to said first processing element, said first processing element sending a signal to said third processing element indicating that said third processing element may access a memory shared between said first processing element and said third processing element.

31. A method for reducing data retrieval latencies in a multiple processing element environment, comprising:

receiving, at a first processing element, update data forwarded from a second processing element, the update data including data relating to operations performed at the second processing element;

retrieving data from the update data in order to execute an instruction at the first processing element; and

revising a subset of the received update data in response to the execution of the instruction on the first processing element.

32. The method of claim 31, further comprising forwarding the revised subset of the update data a third processing element.

33. The method of claim 31, further comprising forwarding a subset of the received update data to a third processing element.

34. The method of claim 31, further comprising generating update data at the second processing element, and forwarding the generated update data to a third processing element.

35. The method of claim 31, wherein the update data is associated with a variable shared by the first processing element and the second processing element.

36. The method of claim 31, wherein the update data includes a memory address that is associated with memory shared by the first processing element and the second processing element.

37. The method of claim 31, further comprising decrementing a time-to-live value associated with the data value.

38. The method of claim 31, further comprising sending a signal from the second processing element to a third processing element indicating that the third processing element

may access a memory shared between the second processing element and the third processing element.

39. A method for forwarding data between processing elements, comprising:

storing a first memory address to an address register at a first processing element;

retrieving a second memory address associated with a second processing element from a forwarding storage element;

comparing the second memory address with the first memory address; and

updating a data register at the first processing element with a data value from the second processing element in response to said comparing.

40. The method of claim 39, wherein the data value is associated with a shared variable.

41. The method of claim 39, wherein the first memory address and the second memory address are associated with memory shared by the first processing element and the second processing.

42. The method of claim 39, further comprising identifying a validity of the data value.

43. The method of claim 39, further comprising decrementing a time-to-live value associated with the data value.

44. The method of claim 39, wherein the data value is associated with a particular network connection record.

45. The method of claim 39, further comprising sending a signal from the second processing element to a third processing element indicating that the third processing element may access a memory shared between the second processing element and the third processing element.